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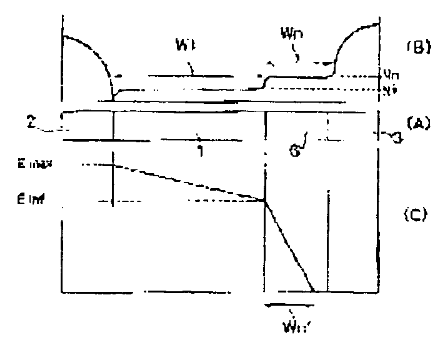
(54) SEMICONDUCTOR ELEMENT AND LIFE TIME CONTROL METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To relax rapid current drop at the time of the end of inverse recovery, and to reduce spike voltage.

SOLUTION: A p type anode layer 2 and an n+ type cathode layer 3 are respectively formed at one edge and the other edge of a substrate constituted of an n type semiconductor whose density is extremely low, and an i layer 1 is formed between the p type anode layer 2 and the n+ type cathode layer 3 in this semiconductor element. An n type impurity layer 6 whose density is lower than that of the n type cathode layer 3 is formed between the i layer 1 and the n+ type cathode layer 3. A distance Wn of the n type impurity layer 6 is made sufficiently shorter than a distance Wi of the i layer 1. Also, the following formula is established by defining the maximum electric field intensity as Emax, and electric field intensity when the inclination of the electric field is changed due to the difference of density of the i layer 1 and the n type impurity layer 6 as Einf, and a distance from the distance Wi when the electric field is turned into 0 as Wn' (Wn'<Wn) for obtaining a design breakdown strength Vb of the semiconductor element. In this formula, Vb=(Emax+Einf)Wi/2+EinfWn'/2.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the semiconductor device and the life-time control method which reduced the electrostatic induction by current reduction and enabled stable operation about the semiconductor device used for a power converter, especially a pin diode.
[0002]
[Description of the Prior Art] A pin diode is the semiconductor device which is widely used for a power converter and can realize high pressure-proofing and a low forward voltage drop.
[0003] Drawing 18 A (outline block diagram) and B (impurity-atom-concentration-profile view) shows explanatory drawing of a pin diode generally known. It is the substrate (generally) to which a sign 2 changes from a very low-concentration n-type semiconductor in drawing 18 . the anode layer (anode field; -- hereafter) which consists of the p type semiconductor prepared in one edge of the substrate which consists of a n-type semiconductor p type anode layer is shown and a sign 3 shows the cathode layer (cathode field; -- n+ type cathode layer is called hereafter) which consists of the comparatively high-concentration n-type semiconductor prepared in the other-end section of the aforementioned substrate A sign 1 shows i layers (intrinsic layer) formed between the aforementioned p type anode layer 2 and n+ type cathode layer 3. The i aforementioned layers of pin diodes are constituted by 1, p type anode layer 2, and n+ type cathode layer 3.
[0004] i layers depletion-ize a pin diode as shown in drawing 18 at the time of reverse voltage impression, and it is obtained in i layers with narrow high voltage at it. In a forward characteristic, a carrier is filled with i narrow layers and a low voltage drop arises.
[0005]
[Problem(s) to be Solved by the Invention] In the reverse-recovery property of the aforementioned pin diode, as shown in the circuit diagram of drawing 19 , when the snubber circuit 5 of owner polarity is connected to a pin diode 4, a property as shown in the current (curve ID) and the voltage (curve VD) wave form chart of drawing 20 is shown. In drawing 20 , it can read that the current in a pin diode is extinguished not continuation (dotted-line section) but suddenly as shown in the portion surrounded with the alternate long and short dash line in the current curve ID (real line part). Diode will be destroyed, when it changes into the state where it was superimposed on the induced voltage of the letter of a spike from the state of high applied voltage and the induced voltage exceeds pressure-proofing by such steep di/dt.
[0006] Drawing 21 shows the reverse-recovery-current (reverse current; anode current) wave form chart to the elapsed time in a pin diode. In addition, the dotted-line section in drawing 21 shows the portion into which a reverse current disappears. In the current curve IA in drawing 21 , the portion to which, as for a points, the forward current is flowing to the pin diode, a portion just before, as for b points, the reverse current of a pin diode disappears, and c points show the portion into which the reverse current of a pin diode disappeared.
[0007] Drawing 22 , and 23 and 24 show a in drawing 21 , b, the concentration-of-electrons distribution map to the distance (distance from the edge by the side of p type anode layer in a pin diode) in c points, a hole concentration distribution map, and a field strength distribution map, respectively. Since the hole concentration in i layers was falling rapidly at the same time the carrier near n+ type cathode layer (an electron and hole) disappears at the time of a reverse-recovery end as shown in drawing 22 and 23, it was made clear that reduction of rapid current as shown in drawing 20 took place.
[0008] Moreover, since electric field (dotted-line section in drawing 24) produce a pin diode in n+ type cathode layer side apart from the electric field by the side of p type anode layer as shown in drawing 24 , and each electric fields by the side of these p type anode layer and n+ type cathode layer overlap mutually, it can read that the carriers by the side of n+ type cathode layer decrease in number rapidly.
[0009] this invention is to accomplish based on the aforementioned technical problem, ease the rapid current fall of the current at the time of a reverse-recovery end, suppress generating of spike voltage, and offer a semiconductor device and the life-time control methods, such as a pin diode in which stable operation is possible.
[0010]
[Means for Solving the Problem] In order to aim at solution of the aforementioned technical problem, this invention the 1st invention While forming the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer It is characterized by preparing the impurity layer which consists of a comparatively low-concentration n-type semiconductor between the aforementioned cathode layer and i layers.
[0011] It is characterized by the aforementioned impurity layer thickness making the 2nd invention thin in the 1st invention of the above as compared with the thickness of the i aforementioned layers.
[0012] The 3rd invention is set to the 1st invention of the above. the specific inductive capacity of epsilon 0 and a semiconductor material for the dielectric constant of vacuum epsilon, Eg and the concentration of the i aforementioned layers for q and a band gap nickel, [the amount of electronic charge] Nn and the aforementioned impurity layer thickness for the concentration of Wi and the aforementioned impurity layer Wn, [the thickness of the i aforementioned layers] The electric field in the aforementioned impurity layer the distance between the portion of 0, and Above Wi Wn', The greatest withstand-voltage value which can obtain the field strength at the time of the inclination of electric field changing the maximum field strength with the concentration differences of Emax, and the i aforementioned layers and n type impurity layer by Einf, and is acquired by Vb and pi junction in design pressure-proofing is set to Vbm. Above Vb 2+EinfWn' [Wi(Emax+Einf) /]/2 and Above Emax The function of the concentration nickel of the i aforementioned layers (2Vbm / (2epsilon0epsilonVbm/qNi) 1/2), Emax-qNiWi/epsilon0epsilon and aforementioned Wn' Above Einf Einf/(qNn/epsilon0epsilon), So that it may be made for Above Vbm to be set to 60(1016-/nickel) 3/4x(Eg/1.1) 3/2 and the distance which lengthened Wn' from Above Wn may thicken as compared with the thickness of the electric field produced in the cathode side of the aforementioned substrate It is characterized by designing the concentration of the i aforementioned layers concentration, thickness, and the aforementioned impurity layer, and thickness.
[0013] While the 4th invention forms the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer It is characterized by preparing two or more steps of impurity layers which consist of a high-concentration n-type semiconductor between the i aforementioned layers and a cathode layer as compared with the concentration of the i aforementioned layers, respectively.

which the aforementioned impurity layer changes from a high-concentration n-type semiconductor in the 4th invention of the above as compared with the concentration nickel of the i aforementioned layers, and the aforementioned 1st impurity layer -- since -- it is characterized by changing

[0015] The 6th invention prepares C steps of aforementioned impurity layers in the 4th invention of the above, and are set concentration of the i aforementioned layers to nickel, and thickness is set to Wi. Electric field [in / x and its x / for the arbitrary distance of the depth direction of a semiconductor device] E (x), It is the following formula and [0016], thickness being set to W (x) and concentration being set to N (x), and the electric field of the impurity layer of a C-flute eye being set to E (c), setting thickness to W (c), and the electric field in the impurity layer of the aforementioned C-flute eye making W(c)' distance between the portion of 0, and Above Wi, and using design pressure-proofing as Vb.

[Equation 4]

$$Vb=\left(\sum_{x=0}^{c-1}\left(E_{(x)}+E_{(x+1)}\right)W_{(x)}+E_{(c)}W_{(c)}'\right)/2$$

[0017] ********** -- while making it like, it is characterized by designing the aforementioned W (x) and N (x), respectively so that the distance which lengthened W[from / aforementioned / W (c)] (c)' may lengthen as compared with the distance of the electric field produced in the aforementioned cathode side

[0018] The 7th invention sets to Vbm the greatest withstand-voltage value from which the specific inductive capacity of epsilon 0 and a semiconductor material can be obtained by epsilon, and the amount of electronic charge is obtained by q and pi junction in the dielectric constant of vacuum in the 6th invention of the above, and, for E (0), (2Vbm / (2epsilon0epsilonVbm/qNi) 1/2), and E (n) and (n!=0) are [0019].

[Equation 5]

$$E_{(0)}-q/\varepsilon_0\varepsilon\times\sum_{x=0}^{n-1}\left(N_{(x)}W_{(x)}\right)$$

[0020] It is characterized by the bird clapper.

[0021] From the distance d0 of a substrate, peak concentration Nn is diffused and two or more aforementioned steps of impurity layers form so that the formula of a concentration distribution may serve as Gaussian distribution in approximation in the above 6th or the 7th invention, and they set to Wd distance between the above d0 and the portion from which the concentration by the aforementioned diffusion becomes the double precision of the concentration nickel which is i layers, and octavus invention is [0022].

[Equation 6]

$$N_{(x)}=Ni+(Nn-Ni)\left(\frac{Ni}{Nn-Ni}\right)^{\frac{(x-d0)^2}{Wd^2}}$$

[0023] ********** -- x [in / the formula of the aforementioned N (x) / it is made like and] is minute -- while setting section **x to W (x) of the formula of the aforementioned design proof pressure Vb -- the above -- minute -- it is characterized by designing Above Nn, d0, and Wd so that the pressure-proofing which asked for the concentration of section **x as N (x) may turn into design pressure-proofing

[0024] While the 9th invention forms the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the life-time control method of the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer By the electric field produced with applied voltage just before a rapid reduction of current takes place, it is characterized by performing electron beam irradiation of comparatively low acceleration voltage from the anode side of the aforementioned substrate so that the life time between aforementioned i layer near ends and cathode layers may be lengthened.

[0025] It is characterized by the 10th invention performing electron beam irradiation of comparatively high acceleration voltage from the cathode side of the aforementioned substrate in the 9th invention of the above instead of performing electron beam irradiation of comparatively low acceleration voltage from the anode side of the aforementioned substrate.

[0026] While the 11th invention forms the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the life-time control method of the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer By the electric field produced with applied voltage just before it irradiates any one kind of charged particle twice [at least] or more to the aforementioned substrate among charged particles, such as an electron ray, a proton, and helium, and a rapid reduction of current takes place It is characterized by controlling to lengthen the life time between i layer near ends and cathode layers.

[0027] The 12th invention is characterized by carrying out multiple-times irradiation of the charged particle of a kind which is different among the charged particles of **, such as the aforementioned electron ray, a proton, and helium, respectively to the aforementioned substrate in the 11th invention of the above.

[0028] The 13th invention is characterized by irradiating the aforementioned charged particle to an anode [of the aforementioned substrate], cathode, or anode side, and a cathode side in the above 11th or the 12th invention.

[0029] While the 14th invention forms the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the life-time control method of the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer By preparing the short layer of a life time in an anode [in the i aforementioned layers], and cathode side, it is characterized by controlling by the electric field produced with applied voltage just before a rapid reduction of current takes place to lengthen the life time between i layer near ends and cathode layers.

[0030] The 15th invention is characterized by applying the life-time control method of the above 9th - the 14th invention in the above 1st - octavus invention.

[0031]

[Embodiments of the Invention] Hereafter, the 1st of operation of this invention - the 11th gestalt are explained based on a drawing.

[0032] The 1st of operation of this invention - the 7th gestalt ease the rapid current fall of the current at the time of a reverse-recovery end, and examine the pin diode which suppressed generating of spike voltage.

[0033] First, drawing 1 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (field strength distribution map at the time of proof-pressure impression) shows explanatory drawing of the pin diode in the 1st gestalt of operation of this invention. in drawing 1 , a sign 6 shows the impurity layer (n+ type cathode layer 3 -- low concentration; -- n type impurity layer is called hereafter) which consists of the n-type semiconductor formed between 1 and n+ type cathode layer 3 i layers

[0034] Here, Wi and its high impurity concentration of i layer 1 are set to nickel for the aforementioned distance [in / 1 / i layers] (thickness), and Wn and its high impurity concentration of n type impurity layer 6 are set to Nn for the distance of the aforementioned n type impurity layer 6. First, in Above Wi and Wn, if Above Wn becomes long (thickly) too much, in order to cause elevation of a forward voltage drop, it is required that Above Wn should be enough shortened compared with Above Wi (thickly). Therefore, in Above Wi and Wn, it is required to realize relational-expression Wi>>Wn.

[0035] Moreover, the design proof pressure Vb of a pin diode needs to be obtained. The field strength produced by impression of reverse voltage can be expressed by Poisson's equation, and when it designs so that pressure-proofing may be determined by the maximum field strength Emax, in a pin diode, the following (1) formula needs to be realized in approximation. In addition, Einf shows ********** at the time of i layers of inclinations of electric field changing with the concentration differences of 1 and n type impurity layer 6. Moreover, Wn' is the distance from Wi at the time of electric field being set to 0, and the Wn' is taken as a short thing as compared with Wn.
[0036]
2+EinfWn' [Vb=(Emax+Einf) Wi/]/2 .... The reason the (1) aforementioned (1) formula needs to be realized is for making it the electric field in pressure-proofing not reach n+ type cathode layer.
[0037] Emax of the aforementioned (1) formula can be expressed with the function of the following nickel. In addition, Vbm shows the greatest withstand-voltage value (the greatest withstand-voltage value acquired by the junction (pi junction) to p type anode layer and i layers) acquired when 1 is long enough i layers.
[0038]
(2Vbm / (2epsilon0epsilonVbm/qNi) 1/2) .... (2) -- again -- Einf -- setting -- Emax-qNiWi/epsilon0epsilon .. (3) Wn' -- setting -- Einf/(qNn/epsilon0epsilon) .. (4) Vbm -- setting -- 60(1016/nickel) 3/4x(Eg/1.1) 3/2 .. It can express (5). In addition, for the above epsilon 0, the dielectric constant of vacuum and epsilon shall be [the amount of electronic charge and Eg of the specific inductive capacity of a semiconductor material and q] band gaps. Moreover, let distance which deducted Wn' from Wn be a long thing as compared with the distance of the electric field produced in a cathode side.
[0039] Next, the 2nd gestalt of operation of this invention is explained. If the ratio of the concentration of Nn and the concentration of nickel is large at the pin diode shown in aforementioned drawing 1 , in junction in 1 and n type impurity layer 6, the same phenomenon as the phenomenon which happens by junction in 1 and n+ type cathode layer 3 i layers as shown in drawing 1 may arise, and i layers of spike voltage may occur. In this case, if concentration of Nn is made thin, Wn will become long and will cause elevation of a forward voltage drop. Then, as shown in the 2nd gestalt of this operation of drawing 2 (a detail is mentioned later), the pin diode of structure which prepared two or more steps of impurity layers between i layers and n+ type cathode layer was examined.
[0040] Drawing 2 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (field strength distribution map at the time of proof-pressure impression) shows explanatory drawing of the pin diode in the 2nd gestalt of this operation. In addition, the same sign is given to what is shown in drawing 1 , and the same thing, and the detailed explanation is omitted.
[0041] In drawing 2 , sign 7a shows 1stn type impurity layer prepared i layers between 1 and n+ type cathode layer 3 (2ndn type impurity layer mentioned later), and high impurity concentration of the 1stn type impurity layer 7a is taken as what [aforementioned] is higher than the high impurity concentration of 1 i layers. sign 7b -- an aforementioned the 1n type -- 2ndn type impurity layer prepared between impurity layer 7a and n+ type cathode layer 3 is shown, and the high impurity concentration of the 2ndn type impurity layer 7b is higher than the high impurity concentration of 1stn type impurity layer 7a, and is taken as a low thing rather than the aforementioned n+ type cathode layer 3 The ratio of the high impurity concentration of aforementioned 1stn type impurity layer 7a and 2ndn type impurity layer 7b is controlled so that spike voltage does not occur.
[0042] Although in the case of the pin diode shown in drawing 2 two steps of n type impurity layers (the 1st, 2ndn type impurity layer) are formed between 1 and n+ type cathode layer 3 and i layers grow into it, elevation of a forward voltage drop can be suppressed more by making these n type impurity layer into two or more steps. For example, it is made for the formula of the following [proof pressure / Vb / at the time of making two or more aforementioned steps of n type impurity layers into a C flute] to be realized.
[0043]
[Equation 7]

$$Vb=\left(\sum_{x=0}^{c-1}(E_{(x)}+E_{(x+1)})W_{(x)}+E_{(c)}W_{(c)}'\right)/2 \qquad \cdots\cdots \quad (6)$$

[0044] In addition, distance which deducted [aforementioned] W(c)' from W (c) is made long as compared with the distance of the electric field produced in a cathode side, and x shows the arbitrary distance of the depth direction of a semiconductor device. Moreover, E (0) can be expressed with the formula (the aforementioned (2) formula) of Above Emax, and can express E (n) and (n!=0) with the following formula.
[0045]
[Equation 8]

$$E_{(0)}-q/\varepsilon_0\varepsilon\times\sum_{x=0}^{n-1}(N_{(x)}W_{(x)}) \qquad \cdots\cdots \quad (7)$$

[0046] Next, the 3rd gestalt of operation of this invention is explained. Drawing 3 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (field strength distribution map at the time of proof-pressure impression) shows explanatory drawing of the pin diode in the 3rd gestalt of this operation. In addition, the same sign is given to what is shown in drawing 1 , and the same thing, and the detailed explanation is omitted. In drawing 3 , broadcloth diffusion by n type impurity is performed to the cathode side of a pin diode, and i layers of n type diffusion layers 8 are formed between 1 and n+ type cathode layer 3. The high impurity concentration of the aforementioned n type diffusion layer 8 can show Gaussian distribution, and can express the Gaussian distribution with the following formula.
[0047]
[Equation 9]

$$N_{(x)}=Ni+(Nn-Ni)\left(\frac{Ni}{Nn-Ni}\right)^{\frac{(x-d0)^2}{Wd^2}} \qquad \cdots\cdots \quad (8)$$

[0048] In addition, if the minute section delta x of x in the aforementioned (8) formula is set to W (x) of the aforementioned (6) formula and high impurity concentration in that case is set to N (x), pressure-proofing can be calculated like the aforementioned (6) formula, and Nn, d0, and Wd will be designed so that the pressure-proofing may turn into design pressure-proofing of a pin diode.
[0049] From the aforementioned (8) formula, when x ared0, N(x) =Nn and a bird clapper can be read. There is no need for d0 above of it being located in a cathode side and being in the interior of an element rather than n-n+ junction (junction in i layers and n+ type cathode layer). Moreover, on the above conditions, it can be made structure which high impurity concentration generally increases one by one to a cathode side. In addition, the dotted-line section in aforementioned drawing 3 shows the impurity atom concentration profile at the time of diffusing an impurity (n type impurity) in consideration of the aforementioned (8) formula, and the impurity atom concentration profile at the time of diffusing n type impurity further is shown in a real line part.
[0050] Next, the 4th gestalt of operation of this invention is explained. Drawing 4 A (outline block diagram), B (impurity-atom-concentration-profile view),

In addition, the same sign is given to what is shown in drawing 1 , and the same thing, and the detailed explanation is omitted. what shows the impurity layer (n- type impurity layer is called hereafter) which consists of the comparatively low-concentration n-type semiconductor which formed the sign 9 between n type impurity layer 6 and n+ type cathode layer 3 in drawing 4 -- it is -- the high impurity concentration of the n- type impurity layer 9 -- the aforementioned n type impurity layer 6 -- low -- a potato's -- ** -- it carries out

[0051] Although i layers high-impurity-concentration Nn- of n- type impurity layer 9 is lower than the high impurity concentration nickel of 1 in the case of the pin diode shown in drawing 4 , as shown, for example in drawing 5 A (outline block diagram) and B (impurity-atom-concentration-profile view), i layers the concentration nickel of 1 and concentration Nn- of n- type impurity layer 9 may be made equal, and a pin diode may be constituted. Moreover, as shown in drawing 6 A (outline block diagram) and B (impurity-atom-concentration-profile view), you may make i layers concentration Nn- of n- type impurity layer 9 higher than the concentration nickel of 1. In addition, although it is satisfactory even if the electric field at the time of the proof-pressure impression in the aforementioned pin diode exist in n type impurity layer 6 or n- type impurity layer 9, it is necessary to make it the electric field and electric field produced from a cathode side not cross.

[0052] Next, the 5th gestalt of operation of this invention is explained. Drawing 7 A (outline block diagram) and B (impurity-atom-concentration-profile view) shows explanatory drawing of the pin diode in the 5th gestalt of this operation. In addition, the same sign is given to what is shown in drawing 2 , and the same thing, and the detailed explanation is omitted. In drawing 7 , a sign 10 shows n- type impurity layer formed between two or more steps of n type impurity layers (the inside of drawing 7 two steps (1stn type impurity layer 7a and 2ndn type impurity layer 7b)) and n+ type cathode layers 3 in a pin diode.

[0053] The high impurity concentration of the aforementioned n- type impurity layer 10 may consider as a low thing rather than the concentration (concentration N (END)) of 2ndn type impurity layer 7b (in the case of a C flute the Cn type impurity layer) which is the last stage among two or more aforementioned steps of n type impurity layers, for example, may be lower than the high impurity concentration nickel of 1 i layers. Moreover, there are two or more aforementioned n- type impurity layers 10, as shown in drawing 8 A (outline block diagram) and B (impurity-atom-concentration-profile view) (the inside of drawing 8 two steps (1stn- type impurity layer 10a and 2ndn- type impurity layer 10b)).

[0054] Next, the 6th gestalt of operation of this invention is explained. Although it indicated that there was no need of d0 being located in a cathode side rather than n-n+ junction, and being located in the interior of an element in the case of the pin diode shown in drawing 3 , it is satisfactory when the d0 is located in an anode side rather than n-n+ junction. For example, as shown in explanatory drawing of the pin diode of drawing 9 A (outline block diagram) and B (impurity-atom-concentration-profile view), when d0 is located in an anode side rather than n-n+ junction, a low portion (sign 11a in drawing 9) is extremely formed rather than the high impurity concentration Nn1 (maximum of the high impurity concentration in n type impurity layer 11) of n type impurity layer 11. Moreover, as shown in drawing 10 A (outline block diagram) and B (impurity-atom-concentration-profile view), when i layers of low n- type impurity layers 12 of high impurity concentration are formed rather than 1 as an extreme example between n type impurity layer 11 in drawing 9 , and n+ type cathode layer 3, the same effect as the pin diode shown in drawing 3 is acquired.

[0055] Next, the 7th gestalt of operation of this invention is explained. Drawing 11 A (outline block diagram) and B (impurity-atom-concentration-profile view) shows explanatory drawing of the pin diode in the 7th gestalt of this operation. In addition, the same sign is given to what is shown in drawing 1 , and the same thing, and the detailed explanation is omitted. In drawing 11 , high impurity concentration differs, respectively and Signs 13a and 13b show the 1st and 2ndn type impurity layer (high-impurity-concentration; 1stn type impurity layer 13a>2ndn type impurity layer 13b) which are formed between 1 and n+ type cathode layer 3 of i layers of lamination of epitaxial growth or a substrate. Signs 14a and 14b -- respectively -- high impurity concentration -- differing -- the lamination of epitaxial growth or a substrate -- an aforementioned the 2n type -- the 1st and 2ndn- type impurity layer (high-impurity-concentration; the 1stn - type impurity layer 14a>2ndn- type impurity layer 14b) which are formed between impurity layer 13b and n+ type cathode layer 3 are shown

[0056] The same effect as the pin diode shown in drawing 3 by the lamination of epitaxial growth or a substrate like the pin diode shown in drawing 11 by forming two or more n type impurity layers and n- type impurity layers with thin concentration between i layers and n+ type cathode layer is acquired. In addition, in a pin diode as shown in drawing 11 , you may form the comparatively deep impurity layer (the inside of drawing 11 1stn type impurity layer 13a, 2ndn- type impurity layer 14b) of concentration formed between i layers and n+ type cathode layer by diffusion.

[0057] Next, how to lengthen the life time near [in a pin diode] n+ type cathode as compared with the life time in fields other than n+ type cathode layer as a method of easing the rapid current fall at the time of the reverse-recovery end in a pin diode is explained.

[0058] Drawing 12 is an absorbed-dose (standardized absorbed dose) distribution property view to the depth in the silicon at the time of thickness carrying out electron beam irradiation with various acceleration energy in the pin diode which is 500 micrometers, and shows the simulation result of the model with which the 90cm air gap existed between an electron gun and silicon (substrate). It has correlation with strong aforementioned absorbed dose and life time, and a life time becomes short, so that the absorbed dose becomes large. Therefore, the life-time distribution to acceleration energy can be read by drawing 12 .

[0059] It can read that take for a life time being so short that it becoming the front face (an irradiation side being called below depth [of 0 micrometer];) of the side in a pin diode irradiated closely when the acceleration voltage of an electron ray is 0.5MeV(s) (curve a) as shown in drawing 12 , and becoming far from the irradiation side, and the influence of the life time by the electron ray is lost. It can read that near 1 a depth of 200 micrometers from the irradiation side in a pin diode takes [the aforementioned acceleration voltage] for a life time's becoming short most and becoming far from near the depth of 200 micrometers in being MeV (curve b), and the life time is long. When the aforementioned acceleration voltage is 2MeV(s) (curve c) and 5MeV (curve d), it can read that it takes for becoming far from the irradiation side in a pin diode, and the life time is short, respectively.

[0060] The octavus gestalt of operation of this invention explains the irradiation method of the electron ray which lengthens the life time near [in a pin diode] n type cathode layer in consideration of the thickness of a pin diode by life-time distribution as shown in drawing 12 .

[0061] The electron-beam-irradiation method in the octavus gestalt of this operation irradiates inside acceleration voltage and the electron ray of low acceleration voltage from the edge by the side of p type anode layer 2 in a pin diode, as shown in drawing 13 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (absorbed-dose distribution map). Or as shown in explanatory drawing of drawing 14 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (absorbed-dose distribution map), you may irradiate inside acceleration voltage or the electron ray of high acceleration voltage from the edge by the side of n+ type cathode layer 3 in a pin diode.

[0062] As shown in drawing 13 and 14, comparatively, the electron ray of low acceleration voltage is irradiated from the edge by the side of p type anode layer 2 in a pin diode, or it becomes possible by irradiating the electron ray of comparatively high acceleration voltage from the edge by the side of n+ type cathode layer 3 in a pin diode to control the life time in a pin diode. In addition, the position which lengthens the life time of the pin diode in the octavus gestalt of this operation is in the electric field produced with applied voltage just before a rapid reduction of current takes place between the end by the side of i layer 1, and n+ type cathode layer 3. Therefore, it is not that what is necessary is just to only lengthen the life time by the side of a cathode with the whole element.

[0063] Although the life-time control method in the octavus gestalt of this operation irradiates an electron ray, or it extends the aforementioned half-value width by high acceleration voltage since half-value width becomes narrow in irradiating charged particles, such as a proton and helium, in addition to the electron ray, the same effect as irradiation of the aforementioned electron ray is acquired by performing irradiation from various directions to an element. Then, in the life-time control method by irradiation of charged particles, such as a proton and helium, the 9th of operation of this invention - the 11th gestalt explain.

[0064] The life-time control method in the 9th gestalt of this operation carries out multiple-times irradiation (compound irradiation) of the charged particle of the same kind from the edge by the side of p type anode layer 2 in a pin diode, as shown in drawing 15 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (absorbed-dose distribution map). In addition, although compound irradiation is performed only from the edge by the side of p type anode layer 2 in the pin diode in the case of the life-time control method shown in drawing 15 , you may perform two aforementioned compound irradiation from a respectively different direction (edge by the side of p type anode layer 2 of a pin diode, and n+ type cathode layer 3) from the edge by the side of n+ type cathode layer [in / a pin diode / for the compound irradiation] 3.

source of irradiation and the source of irradiation is made to intervene, and it is carried out by adjusting various thickness of the board. In that case, in the electric field produced with applied voltage just before a rapid reduction of current takes place, the absorbed dose of the end by the side of i layer 1 and the field between three layers of n+ type cathodes designs a pin diode so that it may decrease from the end by the side of the i layer 1 as compared with portions other than the field between n+ type cathode layers 3.
[0066] The life-time control method in the 10th gestalt of this operation carries out compound irradiation of the charged particles (a proton, helium, etc.) of a kind which is different, respectively from the edge by the side of p type anode layer 2 in a pin diode, as shown in drawing 16 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (absorbed-dose distribution map). In addition, although compound irradiation is performed only from the edge by the side of p type anode layer 2 in the pin diode in the case of the life-time control method shown in drawing 16 , you may perform the edge by the side of n+ type cathode layer [in / a pin diode / for the compound irradiation] 3, or compound irradiation from a respectively different direction (edge by the side of p type anode layer 2 of a pin diode, and n+ type cathode layer 3).
[0067] In order to adjust the irradiation depth in the aforementioned compound irradiation, change acceleration voltage, or the board which consists of silicon or aluminum between the source of irradiation and an irradiated object is made to intervene, and it is carried out by adjusting various thickness of the board. In that case, in the electric field produced with applied voltage just before a rapid reduction of current takes place, the absorbed dose of the field between the end by the side of i layer 1 and n+ type cathode layer 3 designs a pin diode so that it may decrease as compared with portions other than the field between the end by the side of the i layer 1, and n+ type cathode layer 3.
[0068] By diffusing lifetime killers, such as gold or platinum, from the edge by the side of p type anode layer 2 in a pin diode except the life-time control method in the 10th gestalt of this operation In the electric field produced with applied voltage just before a rapid reduction of current takes place, the same effect as the irradiation method in the 10th gestalt of this operation is acquired also in the method of lengthening the life time of the field between the end by the side of i layer 1, and n+ type cathode layer 3.
[0069] Next, the life-time control method in the 11th gestalt of operation of this invention is explained based on explanatory drawing of drawing 17 A (outline block diagram), B (impurity-atom-concentration-profile view), and C (absorbed-dose distribution map). In addition, the same sign is given to what is shown in drawing 13 , and the same thing, and the detailed explanation is omitted.
[0070] The carrier distribution at the time of the flow in a pin diode is determined by the concentration of the anode layer used as the source of supply of a hole, the concentration of the cathode layer used as an electronic source of supply, and the life time. Then, as are shown in drawing 17 , and a charged particle is irradiated from the edge by the side of p type anode layer 2 in a pin diode, and the edge by the side of n+ type cathode layer 3 and the absorption distribution curve alpha of a charged particle shows By preparing the short layer of a life time in p type anode layer [of a pin diode / in / 1 / i layers] 2, and n+ type cathode layer 3 side, respectively, the high impurity concentration of i layer 1 between these two short layers of a life time becomes low. In addition, the curve beta in drawing 17 shows a carrier concentration distribution in case the carrier concentration distribution at the time of a flow and Curve gamma do not perform the aforementioned life-time control.
[0071] In the electric field produced with applied voltage just before a rapid reduction of current takes place, the position and intensity of charged-particle irradiation from the edge by the side of p type anode layer 2 of the aforementioned pin diode and the edge by the side of n+ type cathode layer 3 are controlled by carrier concentration distribution as shown in drawing 17 so that the carrier concentration of the field between the end by the side of i layer 1 and n+ type cathode layer 3 becomes high. As mentioned above, the reverse recovery current in a pin diode is controllable good by controlling the position and intensity of charged-particle irradiation.
[0072] In the pin diode by the 1st of this operation - the 7th gestalt, by applying the control method of a life time shown in the octavus of this operation - the 11th gestalt, design pressure-proofing and the induced voltage by the steep current reduction at the time of a reverse recovery can be reduced more, and the effect of stabilizing operation of a pin diode more is acquired from having been shown above.
[0073]
[Effect of the Invention] As shown above, in the state where there is almost no increase of a forward voltage drop according to this invention, the steep current reduction at the time of design pressure-proofing and a reverse recovery can be eased more effectively, the induced voltage by the current reduction can be reduced, and operation of the stable diode can be realized. Such an effect is acquired when a diffusion process is used.

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] While forming the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer The semiconductor device characterized by preparing the impurity layer which consists of a low-concentration n-type semiconductor between the aforementioned cathode layer and i layers as compared with the aforementioned cathode layer.
[Claim 2] The aforementioned impurity layer thickness is a semiconductor device according to claim 1 characterized by making it thin as compared with the thickness of the i aforementioned layers.
[Claim 3] epsilon and the amount of electronic charge for the specific inductive capacity of epsilon 0 and a semiconductor material q, [the dielectric constant of vacuum] nickel and the thickness of the i aforementioned layers for Eg and the concentration of the i aforementioned layers Wi, [a band gap] Electric field [in / Wn and the aforementioned impurity layer / for Nn and the aforementioned impurity layer thickness / in the concentration of the aforementioned impurity layer] the distance between the portion of 0, and Above Wi Wn', The field strength at the time of the inclination of electric field changing the maximum field strength with the concentration differences of Emax, and the i aforementioned layers and n type impurity layer Einf, The greatest withstand-voltage value acquired by junction to Vb, the aforementioned anode layer, and i layers in design pressure-proofing is set to Vbm. Above Vb 2+EinfWn' [Wi (Emax+Einf) /]/2 and Above Emax The function of the concentration nickel of the i aforementioned layers (2Vbm / (2epsilon0epsilonVbm/qNi) 1/2), Emax-qNiWi/epsilon0epsilon and aforementioned Wn' Above Einf Einf/(qNn/epsilon0epsilon), So that it may be made for Above Vbm to be set to 60(1016-/nickel) 3/4x(Eg/1.1) 3/2 and the distance which lengthened Wn' from Above Wn may thicken as compared with the thickness of the electric field produced in the cathode side of the aforementioned substrate The semiconductor device according to claim 1 characterized by designing the concentration of the i aforementioned layers concentration, thickness, and the aforementioned impurity layer, and thickness.
[Claim 4] While forming the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer The semiconductor device characterized by preparing two or more steps of impurity layers which consist of a high-concentration n-type semiconductor between the i aforementioned layers and a cathode layer as compared with the concentration of the i aforementioned layers, respectively.
[Claim 5] the 1st impurity layer to which the aforementioned impurity layer changes from a high-concentration n-type semiconductor as compared with the concentration nickel of the i aforementioned layers, and the 2nd impurity layer which consists of a high-concentration n-type semiconductor as compared with the aforementioned 1st impurity layer -- since -- the semiconductor device according to claim 4 characterized by changing
[Claim 6] Prepare C steps of aforementioned impurity layers, and are set concentration of the i aforementioned layers to nickel, and thickness is set to Wi. Electric field [in / x and its x / for the arbitrary distance of the depth direction of the aforementioned substrate] E (x), It is the following formula, thickness being set to W (x) and concentration being set to N (x), and the electric field of the impurity layer of a C-flute eye being set to E (c), setting thickness to W (c), and the electric field in the impurity layer of the aforementioned C-flute eye making W(c)' distance between the portion of 0, and Above Wi, and using design pressure-proofing as Vb. [Equation 1]

$$Vb=\left(\sum_{x=0}^{c-1}\left(E_{(x)}+E_{(x+1)}\right)W_{(x)}+E_{(c)}W_{(c)}'\right)/2$$

********** -- the semiconductor device according to claim 4 characterized by designing the aforementioned W (x) and N (x), respectively so that the distance which lengthened W[from / aforementioned / W (c)] (c)' may lengthen as compared with the distance of the electric field produced in the aforementioned cathode side, while making it like
[Claim 7] For E (0), (2Vbm / (2epsilon0epsilonVbm/qNi) 1/2), and E (n) and (n!=0) are, using as Vbm the greatest withstand-voltage value which can obtain the specific inductive capacity of epsilon 0 and a semiconductor material by epsilon, and is acquired [dielectric constant of vacuum] by junction to q, the aforementioned anode layer, and i layers in the amount of electronic charge in a semiconductor device according to claim 6. [Equation 2]

$$E_{(0)}-q/\varepsilon_0\varepsilon\times\sum_{X=0}^{n-1}\left(N_{(x)}W_{(x)}\right)$$

The semiconductor device characterized by the bird clapper.
[Claim 8] From the distance d0 of a substrate, peak concentration Nn is diffused, two or more aforementioned steps of impurity layers form so that the formula of a concentration distribution may serve as Gaussian distribution in approximation, and distance between the above d0 and the portion from which the concentration by the aforementioned diffusion becomes the double precision of the concentration nickel which is i layers is set to Wd. [Equation 3]

$$N_{(x)}=Ni+(Nn-Ni)\left(\frac{Ni}{Nn-Ni}\right)^{\frac{(x-d0)^2}{Wd^2}}$$

********** -- x [in / the formula of the aforementioned N (x) / it is made like and] is minute -- while setting section **x to W (x) of the formula of the aforementioned design proof pressure Vb -- the above -- minute -- the semiconductor device according to claim 6 or 7 characterized by designing Above Nn, d0, and Wd so that the pressure-proofing which asked for the concentration of section **x as N (x) may turn into design pressure-proofing
[Claim 9] While forming the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the life-time control method of the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer The life-time control method characterized by performing electron beam irradiation of comparatively low acceleration voltage from the anode

between aforementioned i layer near ends and cathode layers may be lengthened.
[Claim 10] The life-time control method according to claim 9 characterized by performing electron beam irradiation of comparatively high acceleration voltage from the cathode side of the aforementioned substrate instead of performing electron beam irradiation of comparatively low acceleration voltage from the anode side of the aforementioned substrate.
[Claim 11] While forming the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the life-time control method of the half-**** element constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer By the electric field produced with applied voltage just before it irradiates any one kind of charged particle twice [at least] or more to the aforementioned substrate among charged particles, such as an electron ray, a proton, and helium, and a rapid reduction of current takes place The life-time control method characterized by controlling to lengthen the life time between i layer near ends and cathode layers.
[Claim 12] The life-time control method according to claim 11 characterized by carrying out multiple-times irradiation of the charged particle of a kind which is different among charged particles, such as the aforementioned electron ray, a proton, and helium, respectively to the aforementioned substrate.
[Claim 13] The aforementioned charged particle is the life-time control method according to claim 11 or 12 characterized by irradiating to an anode [of the aforementioned substrate], cathode, or anode side, and a cathode side.
[Claim 14] While forming the anode layer which consists of a p type semiconductor in one edge of the substrate which consists of a low-concentration n-type semiconductor In the life-time control method of the semiconductor device constituted by forming in the other-end section of the aforementioned substrate the cathode layer which consists of a comparatively high-concentration n-type semiconductor, and forming i layers between the aforementioned anode layer and a cathode layer By the electric field produced with applied voltage just before a rapid reduction of current takes place by preparing the short layer of a life time in an anode [in the i aforementioned layers], and cathode side The life-time control method characterized by controlling to lengthen the life time between i layer near ends and cathode layers.
[Claim 15] The semiconductor device characterized by applying the life-time control method according to claim 9 to 14 in a semiconductor device according to claim 1 to 8.

[Translation done.]